Remarks

In response to the Office Action mailed July 14, 2004, Applicants respectfully request reconsideration of the pending claims. To further prosecution of this application, Applicants submit the above amendments.

Claims 1, 2, 4, 7-18, 20-32, 35, 36, 40-45, 47, and 48 are currently pending in the application. Claims 1, 2, 7-12, 14, 16-18, 20-22, 32, 35, 36, 40-43, and 45 stand rejected under 35 U.S.C. §102(b) as anticipated by Bates et al. (US 5,049,978). Claims 13, 15, 44, 47, and 48 stand rejected under 35 U.S.C. §103(a) as unpatentable over Bates et. al in view of Mahulikar et al. (US 5,629,835). Claim 4 stands rejected under 35 U.S.C. §103(a) as unpatentable over Bates et al. in view of Yoshida et al. (JP 59-145537) of Oji et al. (JP 58-197857).

Below, we argue that claims 32 and 45 distinguish over the cited art on the basis of the requirement for a planarizing material filling the recess. We further argue that claims 1, 14, 16, 21, and 45 as amended to include a dielectric material or layer of insulation filling the recess not occupied by the device and conductive bonding material distinguish over the cited art. Support for the amendments may be found on page 3, line 14, page 5, lines 13-14, and page 7, line 6, as well as in Figures 1 and 5. In addition, claims 13, 15, and 47 are further distinguished on the basis of lack of motivation to combine cited reference.

Claims 32 and 40 are allowable over the art of record.

Claim 32 is directed to an electronic component having a non-molded electronic package having a package top and formed from an integral silicon wafer including a

recess, a bare die electronic device where the device is disposed in the recess and physically coupled to the package by a conductive bonding material, and a planarizing material filling the recess not occupied by the device and conductive bonding material to create a level plane that includes the package top. In contrast, Bates et al. leaves a gap around the perimeter of a chip between a substrate and the chip. This difference may be seen from comparison of Figure 1 of the application with Figure 1 of Bates et al., reproduced below.

Application

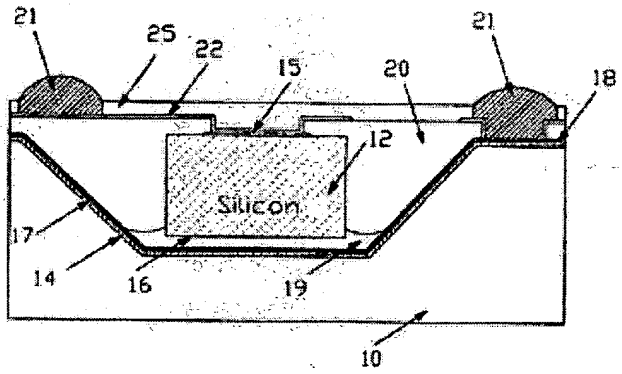
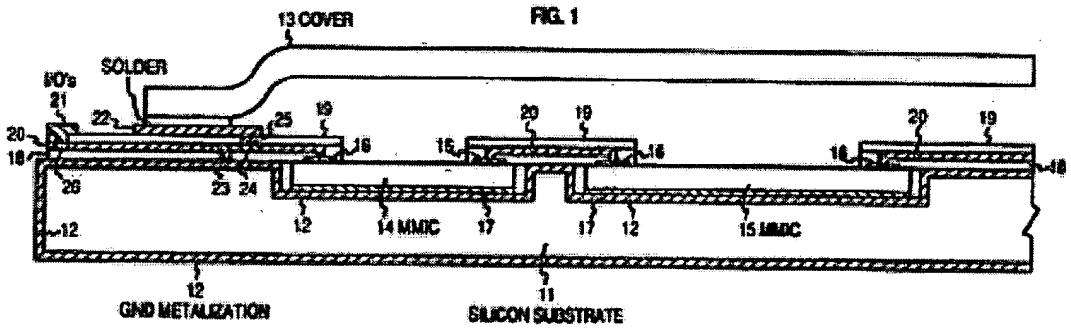


Figure - 1

Bates et al., U.S. 5,049,978



Bates et al. describe an integrated circuit assembly where a MMIC chip is mounted in a recess etched in a silicon substrate such that the top of the chip is planar with the unetched upper surface of the silicon substrate. Bates et al. further present the desirability of retaining a minimum gap between the chip and the substrate to "facilitate bridging of the gap by the thin dielectric layer 18." (See Bates et al., column 5, lines 8-9.) During the interconnection process, all substantially coplanar upper surfaces of the substrate and chips are spray coated with adhesive and a "continuous precast sheet of a polyimid siloxane is placed over the adhesive layer and bonded to the substrate and chips." (See Bates et al., column 6, line 67-column 7, line 6.) Neither the adhesive nor the sheet fills the gap. Planarizing results from the sheet bridging the gap and not from filling the gap.

As Bates et al. does not teach or suggest a planarizing material filling a recess not occupied by a device, claim 32 is distinguishable from the cited art and is in condition for allowance. Claim 40 similarly requires a planarizing material filling the recess not occupied by a device and is also in condition for allowance. Claims 35-36 and 43-44 dependent from claim 32 are allowable for at least the same reasons.

Claims 1, 14, 16, 21, and 45 as amended are allowable over the art of record.

Claim 1 is directed to an electrical component having an electronic device package at least formed from an integral silicon wafer having a recess with a single conductive region, a bare die electronic device disposed in the recess, and a dielectric material disposed to form a planar surface over the recess. In addition, claim 1 requires

that the dielectric material fill the recess not occupied by the device and conductive bonding material.

In view of the teaching of Bates et al. to leave a gap between the chip and the substrate, as discussed above in the context of claim 32, claim 1 is distinguishable from the cited art and is in condition for allowance. Claims 14 and 45 require the dielectric material to fill the recess unoccupied by the device and conductive bonding material with dielectric material and claims 16 and 21 requiring filling of the recess unoccupied by the device and conductive bonding material with a layer of insulation are allowable for the same reasons. Claims 2, 4, 7-13, and 41 dependent from claim 1, claim 15 dependent from claim 14, claims 17-18, 20, and 42 dependent from claim 16, claim 22 dependent from claim 21, and claims 47-48 dependent from claim 45 are allowable for at least the same reasons.

Further distinguishing claims 13, 15, and 47 over the art of record.

Claim 13 is directed to an electronic component comprising an electronic device package formed from an integral silicon wafer having a recess, a bare die electronic device disposed in the recess, a dielectric material filling the recess not occupied by the device and conductive bonding material, a plurality of contacts, and a second layer of dielectric completely covering the silicon wafer and the device except for the plurality of contacts.

There is no motivation to modify the assembly of Bates et al. to include the layer of Mahulikar et al. The cover 13 of Bates et al. already provides the equivalent protection to the substrate.

Claim 15 is directed to an electronic component comprising an electronic component package formed from an integral silicon wafer having a recess, a bare die electronic device having a top terminal electrically coupled to a second conductive region, disposed in the recess, and physically coupled to the package by a conductive bonding material, a dielectric material disposed over the recess and filling the recess not occupied by the device and the conductive bonding material, wherein the second conductive region is a solder bump.

There is no motivation to modify the assembly of Bates et al. to include the solder balls of Mahulikar et al. The assembly of Bates et al. contains a cover 13 that precludes mounting of the assembly in a flip-chip mode. The cover prevents solder balls from contacting a printed circuit board on which the assembly is to be mounted.

Claim 47 is directed to an electronic component comprising a silicon wafer having a recess, a bare die electronic device, and a dielectric material disposed so as to form a planar surface over the recess wherein the bare die electronic device is covered by the dielectric material and the electronic component is a flip chip.

There is no motivation to modify the assembly of Bates et al. to allow it to be mounted as a flip chip. The cover 13 prevents such a mode of mounting.

In view of the foregoing amendments and remarks, this application is now in condition for allowance, and a notice to this effect is respectfully requested. If the Examiner believes, after these amendments, that the application is not in condition for

allowance, the Examiner is invited to call the Applicant's attorney at the number listed below.

Respectfully submitted,

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